IN THE CLAIMS

Below is a copy and status of the pending claims. Please amend claims 4 and 14, as follows:

Claims 1-3 (Canceled)

4. (Currently amended) A circuit comprising:

a voltage node;

a ground node; and

a transistor including a gate, a drain, and a source, the gate being coupled to the voltage node and the drain and source being coupled to the ground node, the transistor ~~operating~~ to operate in the depletion mode wherein the transistor is to remove charge at a constant rate for a non-linear voltage variation, the gate comprising a p-type polysilicon, wherein the transistor has a variable capacitance characteristic that is capable of decreasing noise signals above an absolute value of an operating voltage value at the voltage node and increasing noise signals below the absolute value of the operating voltage value.

5. (Original) The circuit of claim 4, wherein the operating voltage value is between about .5 volts and about 1.5 volts.

6. (Original) The circuit of claim 5, further comprising:

a logic cell coupled to the voltage node and located in close proximity to the transistor.

Claims 7-8 (Canceled)

9. (Previously amended) A circuit comprising:

a die having a high power supply voltage node and a low power supply voltage node; and

a transistor coupled between the high power supply voltage node and the low power supply voltage node and operable for controlling a voltage at the low power supply voltage node.

10. (Previously amended) The circuit of claim 9, wherein the transistor has a gate, a drain, and a source, and the gate is coupled to the high power supply voltage node and the source and the drain are coupled to the low power supply voltage node.

Claims 11-13 (Canceled)

14. (Currently amended) A circuit comprising:

a die;

a ground node located on the die;

a power supply voltage node located on the die; and

an electronic device having a variable capacitance characteristic and that is permanently coupled between the ground node and the power supply voltage node and capable of providing a removal of charge at a constant rate for an asymmetrical ~~response to~~ incremental voltage variations about an operational node voltage at the power supply voltage node.

15. (Original) The circuit of claim 14, wherein incremental voltage variations of one polarity are damped and incremental voltage variations of the opposite polarity are amplified.

16. (Previously amended) The circuit of claim 14, wherein the operational node voltage is about 1.3 volts.

Claims 17-28 (Canceled)